Project Plan
High-Resolution ADC Using Delta-Sigma Architectures
Version 1

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1.3 List of Definitions

Integrated circuit (IC) – an electronic circuit formed on a piece of semiconducting material.[1]

Analog to digital converter (ADC) – an electronic device that converts an analog signal to a digital signal without altering its essential content.[2]

Throttle – control the operation speed of a circuit, and therefore its heat dissipation rate.

Sample – reduce a continuous-time signal to a discrete-time signal by collecting a series of its values at regularly spaced intervals.[3]

Resolution – the number of discrete output values an ADC can produce over the range of analog input values.[4]

Delta-sigma ADC – an ADC that produces a high-resolution output signal using oversampling techniques.[5]

DAC – an electronic device that converts a digital signal to an analog signal without altering its essential content.[6]

Modulator – an electronic device that varies one or more properties of a periodic waveform.[7]

Digital Filter – a system that performs mathematical operations on a discrete-time signal to modify certain aspects of that signal.[8]

Digital Decimator – a device that reduces the sampling rate of a digital signal.[9]

Parasitic Capacitance – a usually unwanted capacitance that exists between parts of electronic components or circuits because of their proximity to each other.[10]

Switched Capacitor Integrator – an electronic device that performs an integrating function using an operational amplifier and a switch-connected capacitor that acts as a current-limiting component.

Comparator – an electronic circuit that compares two voltages and outputs a digital signal indicating which voltage is larger.[11]

Layout – a representation of an integrated circuit using geometric shapes that correspond to the patterns of the materials that make up the physical integrated circuit.[12]

2 Introductory Material

2.1 Acknowledgement

This research and design is greatly supported by Dr. Randall Geiger. We'd like to thank Dr. Geiger for providing and continuing to provide key insight and expertise that greatly assists our research. His contributions are crucial in ensuring our team fully comprehends the scale and knowledge of this project.

2.2 Problem Statement

We rely heavily on various integrated circuits (IC) to perform as originally intended every day. Without these circuits, we would have a difficult time with typical day to day tasks. Heat can become a serious issue when talking about ICs. When these chips overheat, it can damage the circuit and cause it malfunction. There is a need for a method to throttle the circuit performance based on its temperature.

Our team has proposed to create an analog-to-digital converter (ADC) with an onboard temperature sensor to accurately display the current temperature of the IC. With this technology, we can monitor the temperature of an IC as it is being used within a system to ensure it doesn't overheat. Based on this reading, the IC would have a system to throttle its performance to allow proper temperature decrease.

2.3 Operating Environment

Our circuit can be implemented with any IC as it is intended to monitor the temperature of that IC. With this, the operating environments will vary depending on the system they are implemented in. For most purposes, this will result in being used in a small, closed off environment.

2.4 Intended Users and Intended Uses

Our product is to be used by IC designers when designing new ICs. They will implement our system onboard the same IC they are currently designing. In addition to the IC designers, the circuit will be used in the field by whomever is assigned to monitor the temperature of the system.

Our product will be used to successfully and easily measure the temperature of an IC. Its output is intended to be monitored by either a person or a computer. Based on the output, the system will change in performance to allow for maximum performance at ideal temperatures or throttled performance when temperatures rise above a certain threshold.

2.5 Assumptions and Limitations

Assumptions:

- Each IC in a complete system is individually monitored

Limitations:

- Area of the layout is no more than 180 µm x 100 µm
- Supply voltage is to be +/- 1.8 V

2.6 Expected End Product and Other Deliverables

The end product will have a full circuit designed within Cadence in a 180 nm process. Included in this will be a full layout and post layout simulation. This will be delivered by the first week of May 2018 so it can be sent out for fabrication.

The end product will be a fully fabricated IC with our ADC and temperature sensor onboard. This will be fabricated by MOSIS over the summer of 2018 to allow ample time to be completed. The fabrication will be completed by August 2018 to allow our team to test for functionality of the physical IC.

The end product will be biased with an external voltage supply either in a lab or a different portion of the system it is being used in. The voltage supply will operate at +/- 1.8 V.

3 Proposed Approach and Statement of Work

3.1 Proposed Approach

- **3.1.1 Functional Requirements:** The design requirement of this ADC is to be able to sample input signal at 1KHz at the minimum and output the converted data in a 16 bit resolution,
- **3.1.2 Constraints Consideration** : During design, the team will be on a time constraint to deliver the design to be fabricated. Also, there will be some area and power requirements that will be discussed with client.
- **3.1.3 Technology Consideration:** Cadence Virtuoso will be the main design software and it will be provided by Electrical and Computer Engineering department at Iowa State University. Moreover, device fabrication, will be done by MOSIS in a 0.5 micron process.
- **3.1.4 Testing Requirements Consideration:** Upon fabrication, the output product will be tested to validate simulation results using standard existing laboratory equipment at Iowa State University.
- **3.1.5 Safety Consideration:**. This design project should not oppose any safety considerations.
- **3.1.6 Previous Work:** High resolution ADCs are very common in very precise measurements applications and research is still going on how to increase the performance of these devices.
- **3.1.7 Possible Risk and Risk Management:** The first possible risk is losing design data due to server crash; therefore, a copy of the design must be in a safe place. The second sort

of risk is device damage due to mishandling. To minimize the risk, we will request a few copies of the design to fabricated.

- **3.1.8 Project Proposed Milestones and evaluation Criteria:** The following step will represent general milestones of the project and the way they will be evaluated:

  * Research Delta Sigma ADC's literature and understand the structure of the design. * * Evaluation: to get a general block diagram of the design.
  * Design ADC using the right architecture. Evaluation: Simulation results.
  * Design DAC using the required resolution. Evaluation: Simulation results.
  * Design the ADC's Modulator. Evaluation: simulation results.
  * Design and test Digital Filter. Evaluation: Simulation results.
  * Design and test the Decimator unit. Evaluation: Simulation results.
  * Assemble all sub part and test for cumulative output results Evaluation: Simulation results.
  * Test and run simulations after extracting parasitics

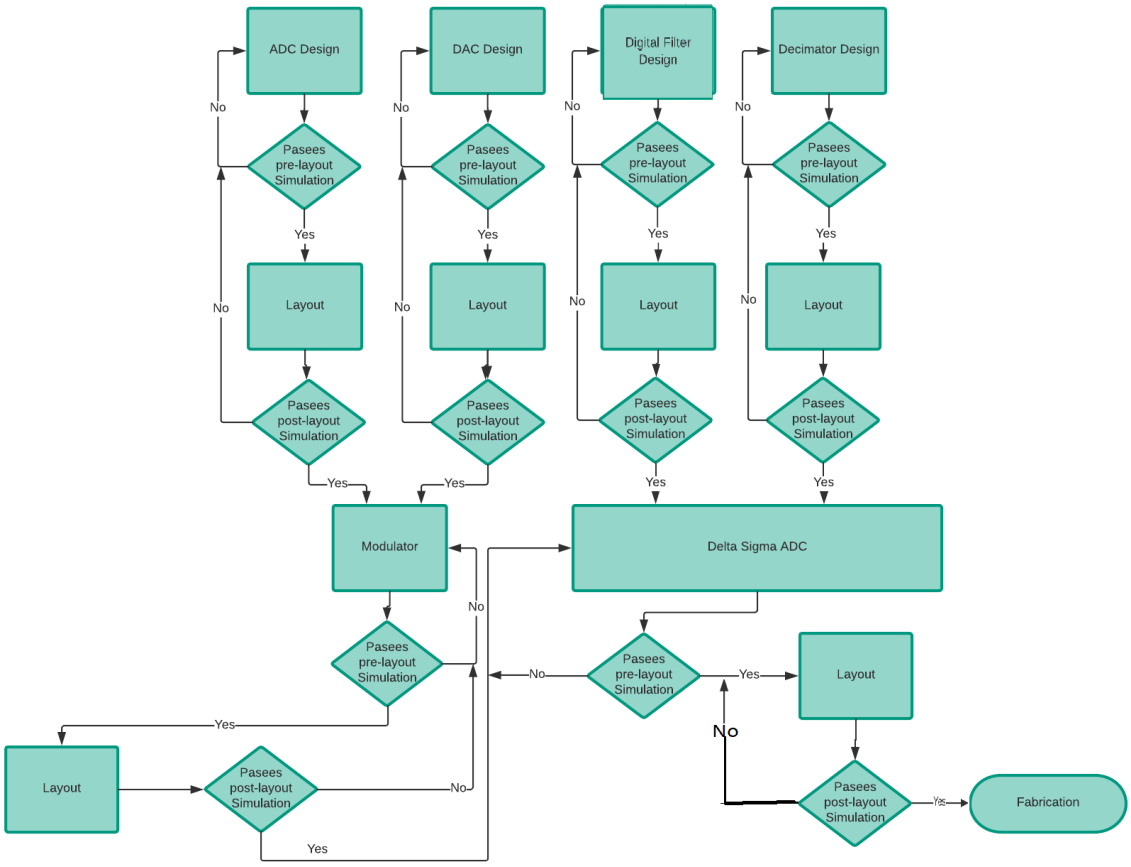

Figure 3.1: Design Process Flow Chart

4 Estimated Resources and Project Timeline

4.1 Personal Effort requirements

Individual Tasks: Temperature Sensor, Switched Capacitor Integrator Filter, Comparator (1-bit ADC), 1-bit DAC, Digital Filter, Digital Decimator

What Needs to be done	How should it be completed	How many hours per week?
Individual Tasks mentioned above	- Each task should be researched deeply. All team members should revise the schematic for each task. - The schematic should be built and simulated - The layout for the schematic should be created - Post-layout simulations should be run	- 10 hours a week should be dedicated during the research and schematic design stage. - 15 hours a week should be dedicated during the schematic simulation stage - 15 hours a week should be dedicated during the layout of the schematic stage - 10 hours a week should be dedicated during the post-layout simulations stage
Testing after combining	1. The switched capacitor integrator circuit combined with both the comparator (1-bit ADC) and the 1-bit DAC should be tested and proven to function optimally together 2. The digital filter and digital decimator should be combined and tested and proven to function optimally together 3. The digital	- 15-20hrs a week dedicated to testing, each time the components are combined and tested together - 20hrs a week dedicated to testing when the final two stages of combination are reached (stage 3 and 4)

	components and the delta sigma modulator should be combined, tested and proven to function optimally together 4. The temperature sensor should be attached at the input of the system and should be tested and proven to function optimally together	
Layout of Individual tasks	1. Each task's layout will be individually designed using Cadence 2. The layouts will be combined 3. Post-layout simulations will be done to ensure no issues exist within the layout	- 15 hours a week will be dedicated to designing the individual task's layout - 10 hours a week will be dedicated to combining the layouts - 20 hours a week will be dedicated to performing post layout simulations
Ensure for fabrication	- Ensure that the circuit will function as intended to the best of our abilities	- 20 hours a week will be dedicated to ensuring that the circuit has no flaws before fabrication
Testing once fabricated	- Performing numerous tests on the fabricated circuit - Trouble shooting the circuit to the best of our abilities	- 15 hours a week will be dedicated to testing and troubleshooting the fabricated circuit
Documentation	- Documenting the project - This will be done on weekly basis throughout the next two semesters	- 10-15 hours a week will be dedicated to documenting the project

Figure 4.1: Project Design Plan

4.2 Resources needed

The resources our team will need include the following: access to Cadence, access to fabrication through MOSIS, access to IEEE libraries and other academic papers.

4.3 Financial Resources needed

Funding to support the fabrication done by MOSIS of the data converter and temperature sensor.

4.4 Project Schedule

	Week of:														
	2/5 - 2/11	2/12 - 2/18	2/19 - 2/25	2/26 - 3/4	3/5 - 3/11	3/12 -3/18	3/19 -3/25	3/26 - 4/1	4/2 - 4/8	4/9 - 4/15	4/16 - 4/22	4/23 - 4/29	4/30 - 5/4	8/20 -12/3	12/3- 12-14
Stage															
Individual Tasks	5 weeks														
Combining Tasks and Testing						4 weeks									
Layout of Individual Tasks										2 weeks					
Ensure For Fabrication												2 weeks			
Testing Post-Fabrication														12 weeks	
Finishing Documentation															2 weeks

Figure 4.2: Project Timeline

5 Closure Materials

5.1 Closing Summary

In an effort to properly design a Delta-Sigma ADC, there are many design and implementation challenges that will be faced. The design must fit the needs of the eventual use case of Drs. Geiger and Chen, and be able to implement itself properly in their larger research needs. They are in need of a high resolution, low latency ADC for the purpose of temperature detection in the circuits they are building. This design approach means adhering to a strict and rigid set of design requirements and considering their needs in the design process. The basic structure of the design will include the delta-sigma modulator, digital filter, and decimator. The modulator will be designed with a difference amplifier, integrator, ADC, and DAC to output to the digital filter. These steps ensure that the design retains a high-resolution element, while being relatively simplistic so to keep budget and time constraints low.

5.2 References

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